REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed March 16, 2004. In the Office Action, the Examiner rejected claims 1-5, 10, 11-15, 20, 21-25 and 30 under 35 U.S.C. §102(b); and claims 6, 16, 26 under 35 U.S.C. §103(a). Reconsideration in light of the remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102

1. In the Office Action, the Examiner rejected claims 1-5, 10, 11-15, 20, 21-25 and 30 under 35 U.S.C. §102(b) as being anticipated over U.S. Patent No. 5,944,815 issued to Witt ("Witt"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of anticipation. As the Examiner may be aware, to anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

Witt discloses a microprocessor configured to execute a prefetch instruction including an access count field defining an expected number of access. A prefetch instruction defines an access count which indicates the number of accesses expected to a cache line (Witt, col. 4, lines 31-34). The data cache preferentially retains the cache line until the access count expires (Witt, col. 5, lines 35-37). A cache line X is "preferentially retained" if cache lines other than X are selected for replacement even if X would be selected according to a replacement algorithm (Witt, col. 5, lines 38-42). A preferentially retained cache line is NOT selected for replacement, even if it is least recently used, if at least one of the other eligible cache line is selectable (i.e., not preferentially retained).

Witt does not disclose, either expressly or inherently, (1) transfer a trace, (2) a first cache to evict the trace based on a replacement mechanism.

PAGE 11/15 * RCVD AT 6/14/2004 6:59:43 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:714 557 3800 * DURATION (mm-ss):04-12

First, Witt merely discloses the access count for use with a data cache, not an instruction cache, or not with a trace cache. Witt specifically discloses an instruction cache and a data cache (Witt, Figure 1, elements 12 and 14) and the use of the access count is associated with only the data cache. In contrast, claims 1, 11, and 21 recite "a trace". A trace is a sequence of instructions that has been executed by the program (See, for example, Specification, page 5, lines 8-16).

Second, Witt merely discloses that a preferentially retained cache lime is NOT selected for replacement. In contrast, claims 1, 11, and 21 recite "a first cache . . . to evict the trace based on a replacement mechanism".

Therefore, not only Witt does not disclose the claimed invention, but also teaches away from the claimed invention. Witt discloses using an access count to keep the cache line in the data cache from being replaced.

Accordingly, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §102(b) be withdrawn.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected claims 6, 16, and 26 under 35 U.S.C. §103(a) as being unpatentable over Witt in view of "Evaluation of Design Options for the Trace Cache Fetch Mechanism", Computers, IEEE Transactions, Volume 48, Issue:2, Feb. 1999 written by Patel et al. ("Patel"), pages: 193-204 and (2) claims 7-9, 17-19, and 27-29 under 35 U.S.C. 1§03(a) as being unpatentable over Witt in view of Patel and further in view of U.S. Patent No. 6,272,598 issued to Arlitt et al. ("Arlitt"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. As the Examiner may be aware, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-124 (8th Ed., rev. 1, Feb. 2003).*

PAGE 12/15 * RCVD AT 6/14/2004 6:59:43 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:714 557 3800 * DURATION (mm-ss):04-12

Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Witt discloses a microprocessor configured to execute a prefetch instruction including an access count field defining an expected number of access as discussed above.

Patel discloses an evaluation of design options for the trace cache fetch mechanism. A trace cache mechanism includes a trace cache, a fill unit, a branch predictor, and an instruction cache. If both the trace cache and instruction cache miss, then a request for the missing instruction cache line is made to the second level cache (Patel, Page 196, right column, third paragraph of section 3.4).

Arlitt discloses a web cache performance by applying different replacement policies to the web cache. A Least Frequently Used (LFU)-Aging replacement policy replaces the least frequently used object, avoiding cache pollution. The LFU component of the replacement policy maintains a frequency count for each object in the cache. The aging component avoids cache pollution by reducing the frequency count of each cached object by a factor of two whenever the average frequency count exceeds a threshold parameter (Arlitt, col. 6, lines 41-49).

Witt, Patel and Arlitt, taken alone or in any combination, does not disclose, suggest, or render obvious (1) transfer of a trace, (2) a first cache to evict the trace based on a replacement mechanism, and (3) a second cache to receive the evicted trace based on a number of accesses to the trace as discussed above. There is no motivation to combine Witt, Patel and Arlitt because none of them addresses the problem of trace cache filtering. There is no teaching or suggestion that a second cache to receive the evicted trace based on number of accesses is present. Witt, read as a whole, does not suggest the desirability of filtering trace cache.

Witt does not disclose any one of the elements recited in independent claims 1, 11, and 21, as discussed above under the 102 rejections. In addition, Patel merely discloses extensions of the trace cache such as partial matching, path associativity, and inactivity (Patel, page 193, right column). Patel merely discloses an L2 cache to fetch missing instruction cache line, not an L2 cache to receive a trace being transferred to the first or second cache for execution as recited in claims 6, 16, and 26. Arlitt merely discloses use of a threshold to reduce the frequency count by two whenever the average frequency count exceeds the threshold. The threshold is used to reduce the frequency count, not to transfer a trace. Furthermore, the threshold is used to

PAGE 13/15 * RCVD AT 6/14/2004 6:59:43 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:714 557 3800 * DURATION (mm-ss):04-12

compare with the average frequency count, not the number of accesses to the trace. In contrast, claims 7, 17, and 27 recite the trace being transferred from the second cache to the L2 cache when a second threshold value is less than a second number of accesses to the trace.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §102(b), and 35 U.S.C. §103(a) be withdrawn.

PAGE 14/15 * RCVD AT 6/14/2004 6:59:43 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:714 557 3800 * DURATION (mm-ss):04-12

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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PAGE 15/15 * RCVD AT 6/14/2004 6:59:43 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:714 557 3800 * DURATION (mm-ss):04-12